Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: B = .006 x .005” E = .005 x .005”**

**Mask Ref: CP310**

**APPROVED BY: DK DIE SIZE .026” X .026” DATE: 11/20/17**

**MFG: CENTRAL SEMI THICKNESS .009” P/N: CZTA44**

**DG 10.1.2**

#### Rev B, 7/1